In the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Claim 1. (Currently amended) A signal generator, comprising:

a voltage controlled oscillation circuit;

a control voltage input terminal for inputting an external control voltage for determining a frequency of an oscillation signal;

a frequency divider circuit for frequency-dividing an oscillation signal output from the voltage controlled oscillation circuit;

a frequency divided signal output terminal for outputting a frequency divided signal output from the frequency divider circuit; and

a buffer amplifier which couples the oscillation signal output of the voltage controlled oscillator circuit to an input of the frequency divider circuit;

wherein the buffer amplifier has a balanced input and an unbalanced output.

Claims 2.- 4. (Canceled)

Claim 5. (Original) The signal generator according to claim 1, wherein the voltage controlled oscillation circuit and the frequency divider circuit are arranged in an integrated circuit, and wherein the integrated circuit is provided with the control voltage input terminal and the frequency division signal output terminal.

Claim 6. (Original) The signal generator according to claim 5, wherein the frequency of oscillation of the voltage controlled oscillation circuit is controlled by a FET functioning as a voltage controlled variable capacitor.

Claim 7. (Original) The signal generator according to claim 5, wherein the integrated circuit is formed utilizing CMOS technology.

Claim 8. (Original) The signal generator according to claim 1, wherein the voltage controlled oscillation circuit employs field effect transistors (FET).

Claim 9. (Original) The signal generator of claim 6, wherein the voltage controlled oscillation circuit has a balanced output.

Claim 10. (Original) The signal generator according to claim 1, further comprising a circuit board on which the voltage controlled oscillation circuit and the frequency divider circuit are provided, wherein the control voltage input terminal and the frequency division signal output terminal are provided on end faces or an underside of the circuit board.

Claim 11. (Original) The signal generator according to claim 1, wherein the voltage controlled oscillator circuit further comprises a varactor diode in a resonant circuit coupled to a base of an oscillating transistor.

Claim 12. (Original) The signal generator according to claim 11, wherein the frequency of oscillation of the voltage controlled oscillation circuit is controlled by the external voltage applied to the varactor diode.

Claim 13. (Original) The signal generator unit of claim 1, wherein a frequency division ratio of the frequency divider circuit is controlled by an externally applied

switching signal.

Claim 14. (Original) The signal generator of claim 1, wherein a frequency division ratio of the frequency divided signal output is a whole number.

Claim 15. (Original) The signal generator of claim 1, wherein a frequency division ratio of the frequency divided signal output is a fractional number.

Claim 16. (Original) The signal generator of claim 1, further comprising a plurality of frequency divider circuits, one or more of the plurality of frequency divider circuits having a corresponding frequency divided signal output terminal.

Claim 17. (Original) The signal generator according to claim 16, wherein the frequency divided signal output from at least two of the plutality of frequency divider circuits are available simultaneously.

Claim 18. (Original) The signal generator according to claim 16, wherein the plurality of frequency divider circuits are connected in series.

Claim 19. (Original) The signal generator according to claim 16, wherein at least one of the plurality of frequency divider circuits is a variable frequency divider circuit capable of switching a frequency division ratio.

Claim 20. (Original) The signal generator according to claim 1, wherein the frequency divided signal output has a frequency that is equal to or lower than the frequency of the oscillation signal.

Claim 21. (Currently amended) A signal generator, comprising:

means for generating an oscillation signal;

means for frequency dividing the oscillation signal; and

means for outputting a frequency divided signal,

wherein a frequency of the oscillation signal is controlled by a first control means and a frequency division ratio of the frequency dividing means is controlled by a second control means; and

wherein the means for generating the oscillation signal comprises:

means for generating a balanced output oscillation signal;

means for converting the balanced output oscillation signal to an unbalanced output oscillation signal; and

means for inputting the unbalanced output oscillation signal to the means for frequency dividing the oscillation signal.

Claim 22. (Canceled)

Claim 23. (Original) The signal generator according to claim 21, wherein the means for frequency dividing the oscillation signal comprises:

means for cascading the means for frequency dividing,

wherein at least one of the cascaded means for frequency dividing is connected to the outputting means.

Claim 24. (Original) The signal generator according to claim 21, wherein the first control means is an externally applied control voltage.

Claim 25. (Original) The signal generator according to claim 21, wherein the second control means is an externally applied switching signal.

Claim 26. (Currently amended) A method of generating a signal with a wide frequency range, comprising:

generating a voltage controlled oscillation signal output;

frequency dividing the voltage controlled oscillation signal output;

controlling a frequency division ratio of the voltage controlled oscillation signal output; and

outputting a frequency divided signal;

wherein the generating a voltage controlled oscillation signal output comprising:

generating a balanced output oscillation signal;

converting the balanced output oscillation signal to an unbalanced output oscillation signal;

controlling a frequency of the balanced output oscillation signal.

Claim 27. (Canceled)

Claim 28. (Currently amended) The method according to claim ~~27~~26, wherein controlling the balanced output oscillation signal comprises applying an external voltage.

Claim 29. (Original) The method according to claim 26, wherein controlling the frequency division ratio comprises applying an external switching voltage.

Claim 30. (New) A signal generator, comprising:

a voltage controlled oscillation circuit;

a control voltage input terminal for inputting an external control voltage for determining a frequency of an oscillation signal;

a frequency divider circuit for frequency-dividing an oscillation signal output from the voltage controlled oscillation circuit;

a frequency divided signal output terminal for outputting a frequency divided signal output from the frequency divider circuit; and

a buffer amplifier which couples the oscillation signal output of the voltage controlled oscillator circuit to an input of the frequency divider circuit;

wherein the buffer amplifier is a common emitter transistor amplifier.

Claim 31. (New) The signal generator according to claim 30, wherein the voltage controlled oscillation circuit and the frequency divider circuit are arranged in an integrated circuit, and wherein the integrated circuit is provided with the control voltage input terminal and the frequency division signal output terminal.

Claim 32. (New) The signal generator according to claim 31, wherein the frequency of oscillation of the voltage controlled oscillation circuit is controlled by a FET functioning as a voltage controlled variable capacitor.

Claim 33. (New) The signal generator according to claim 31, wherein the integrated circuit is formed utilizing CMOS technology.

Claim 34. (New) The signal generator according to claim 30, wherein the voltage controlled oscillation circuit employs field effect transistors (FET).

Claim 35. (New) The signal generator of claim 32, wherein the voltage controlled oscillation circuit has a balanced output.

Claim 36. (New) The signal generator according to claim 30, further comprising a circuit board on which the voltage controlled oscillation circuit and the frequency divider circuit are provided, wherein the control voltage input terminal and the frequency division signal output terminal are provided on end faces or an underside of the circuit board.

Claim 37. (New) The signal generator according to claim 30, wherein the voltage controlled oscillator circuit further comprises a varactor diode in a resonant circuit coupled to a base of an oscillating transistor.

Claim 38. (New) The signal generator according to claim 37, wherein the frequency of oscillation of the voltage controlled oscillation circuit is controlled by the external voltage applied to the varactor diode.

Claim 39. (New) The signal generator unit of claim 30, wherein a frequency division ratio of the frequency divider circuit is controlled by an externally applied switching signal.

Claim 40. (New) The signal generator of claim 30, wherein a frequency division ratio of the frequency divided signal output is a whole number.

Claim 41. (New) The signal generator of claim 30, wherein a frequency division

ratio of the frequency divided signal output is a fractional number.

Claim 42. (New) The signal generator of claim 30, further comprising a plurality of frequency divider circuits, one or more of the plurality of frequency divider circuits having a corresponding frequency divided signal output terminal.

Claim 43. (New) The signal generator according to claim 42, wherein the frequency divided signal output from at least two of the plutality of frequency divider circuits are available simultaneously.

Claim 44. (New) The signal generator according to claim 42, wherein the plurality of frequency divider circuits are connected in series.

Claim 45. (New) The signal generator according to claim 42, wherein at least one of the plurality of frequency divider circuits is a variable frequency divider circuit capable of switching a frequency division ratio.

Claim 46. (New) The signal generator according to claim 30, wherein the frequency divided signal output has a frequency that is equal to or lower than the frequency of the oscillation signal.